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(54) **REPACKAGED INTEGRATED CIRCUIT AND ASSEMBLY METHOD**

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CPC . H01L 2224/05644; H01L 2224/05655; H01L 2224/05664; H01L 2924/15153

See application file for complete search history.

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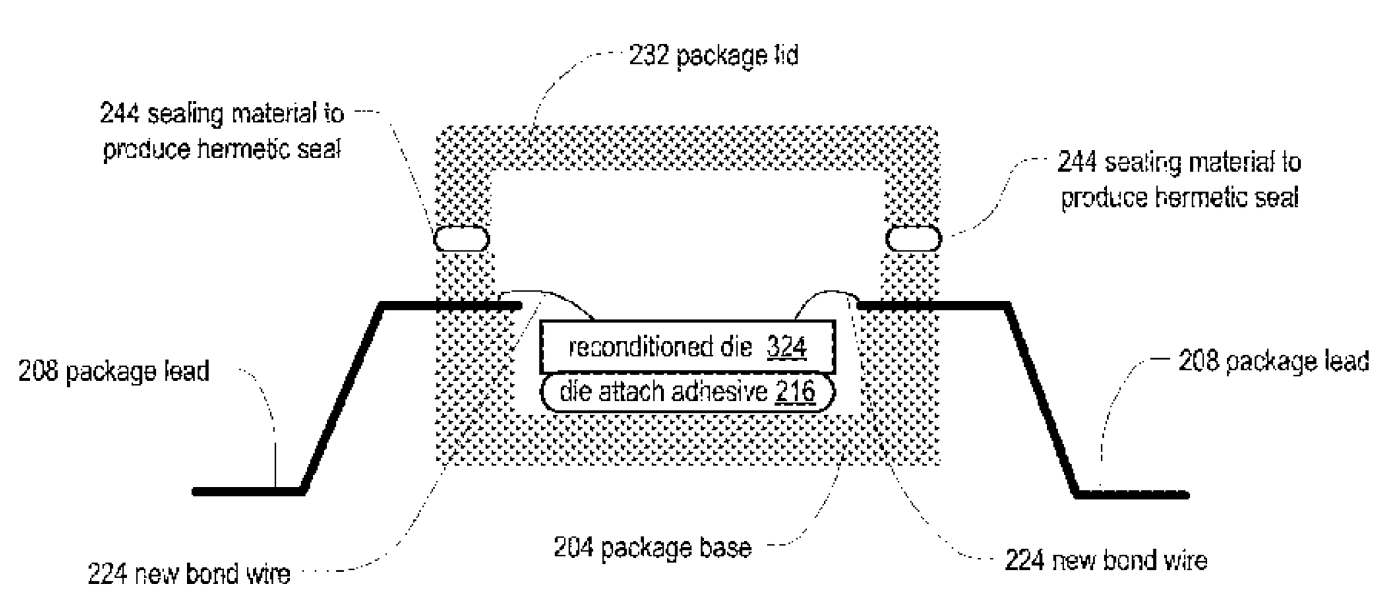
(57) **ABSTRACT**

A packaged integrated circuit for operating reliably at elevated temperatures is provided. The packaged integrated circuit includes a reconditioned die, which includes a fully functional semiconductor die that has been previously extracted from a different packaged integrated circuit. The packaged integrated circuit also includes a hermetic package comprising a base and a lid and a plurality of bond wires. The reconditioned die is placed into a cavity in the base. After the reconditioned die is placed into the cavity, the plurality of bond wires are bonded between pads of the reconditioned die and package leads of the hermetic package base or downbonds. After bonding the plurality of bond wires, the lid is sealed to the base.

12 Claims, 11 Drawing Sheets

Repackaged environmentally hardened integrated circuit 408



Related U.S. Application Data

application No. 13/283,293, filed on Oct. 27, 2011, now abandoned.

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H01L 21/66 (2006.01)
H01L 23/00 (2006.01)
H01L 23/26 (2006.01)

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FIG. 1 Extracted die with bond pads and ball bonds

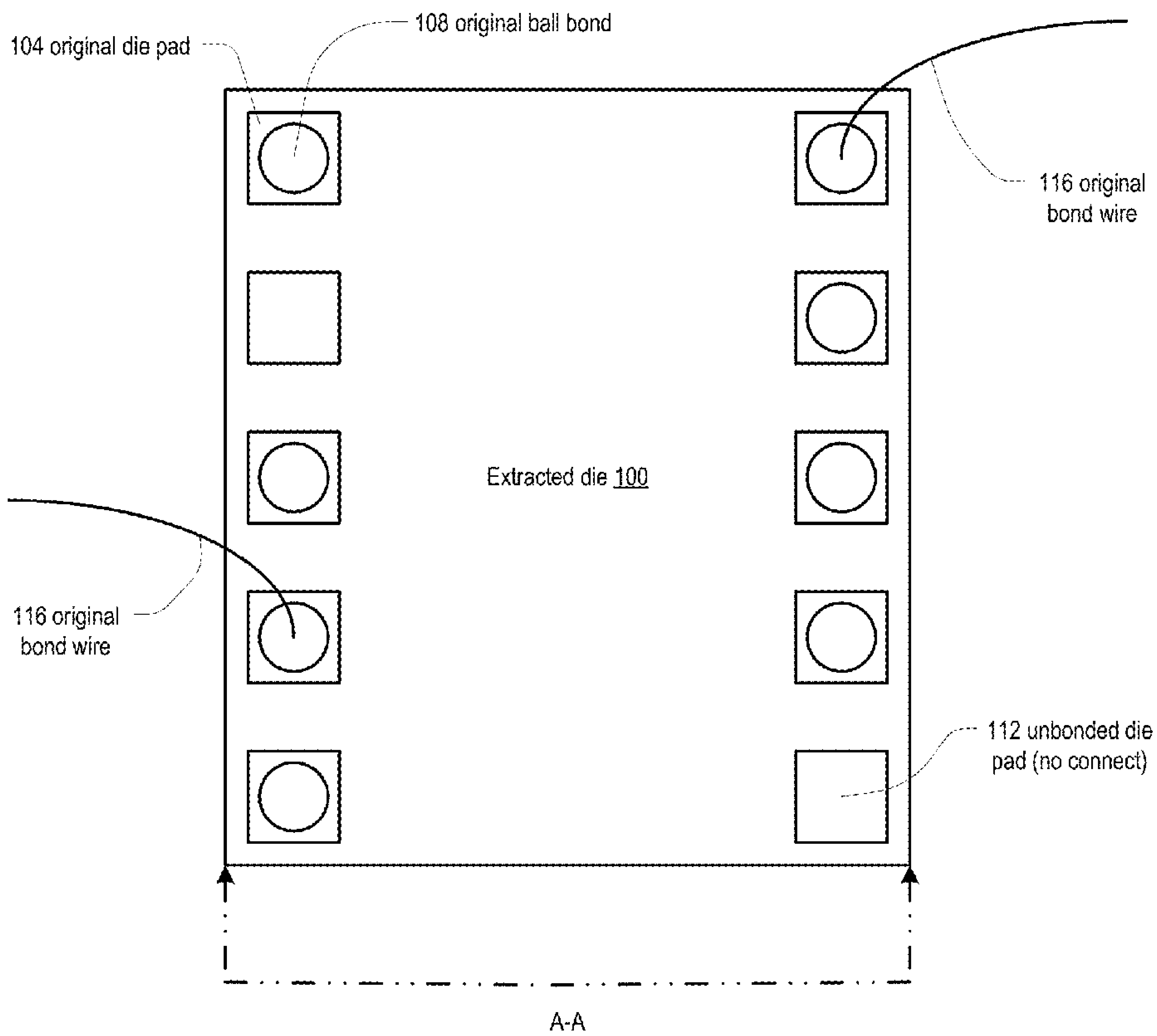


FIG. 2A Extracted die installed in hermetic package base

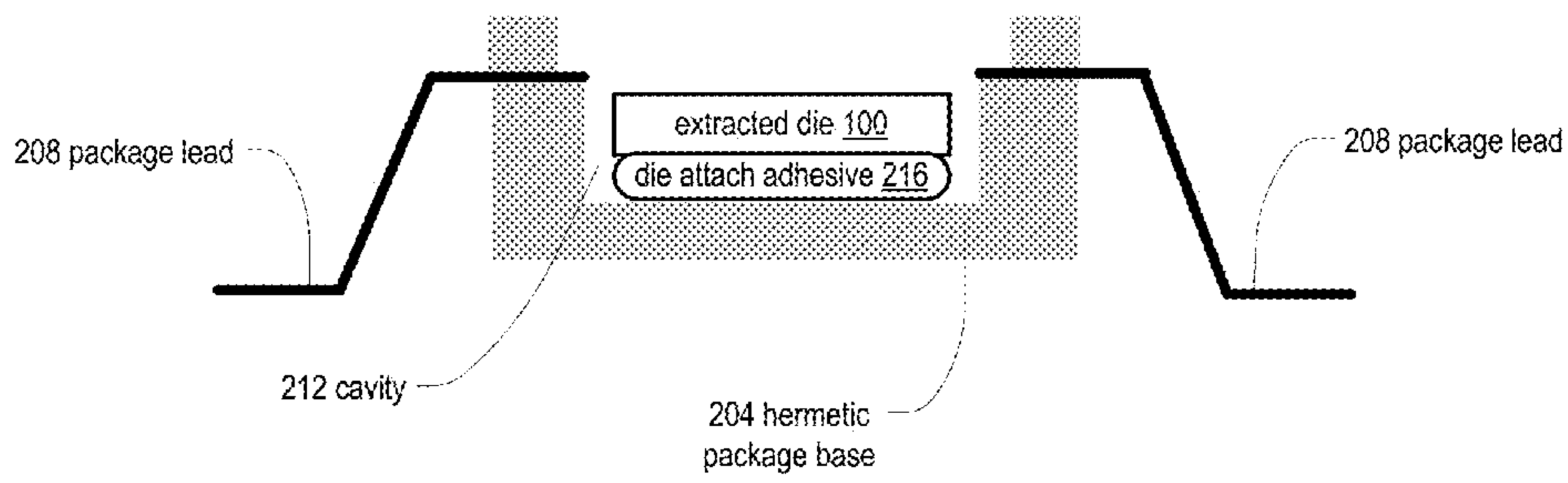


FIG. 2B Extracted die rebonded to a hermetic package base

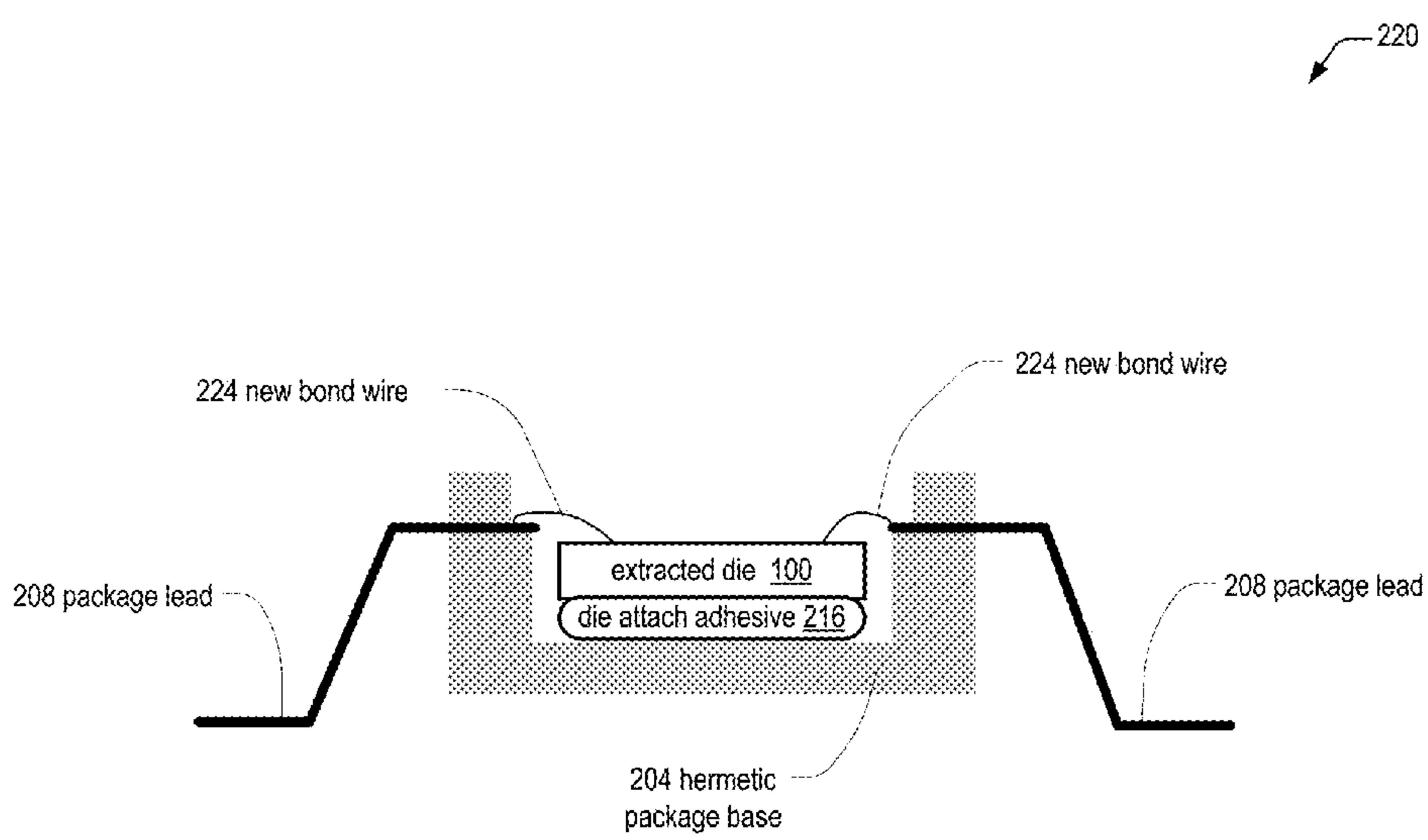


FIG. 2C Repackaged environmentally hardened integrated circuit

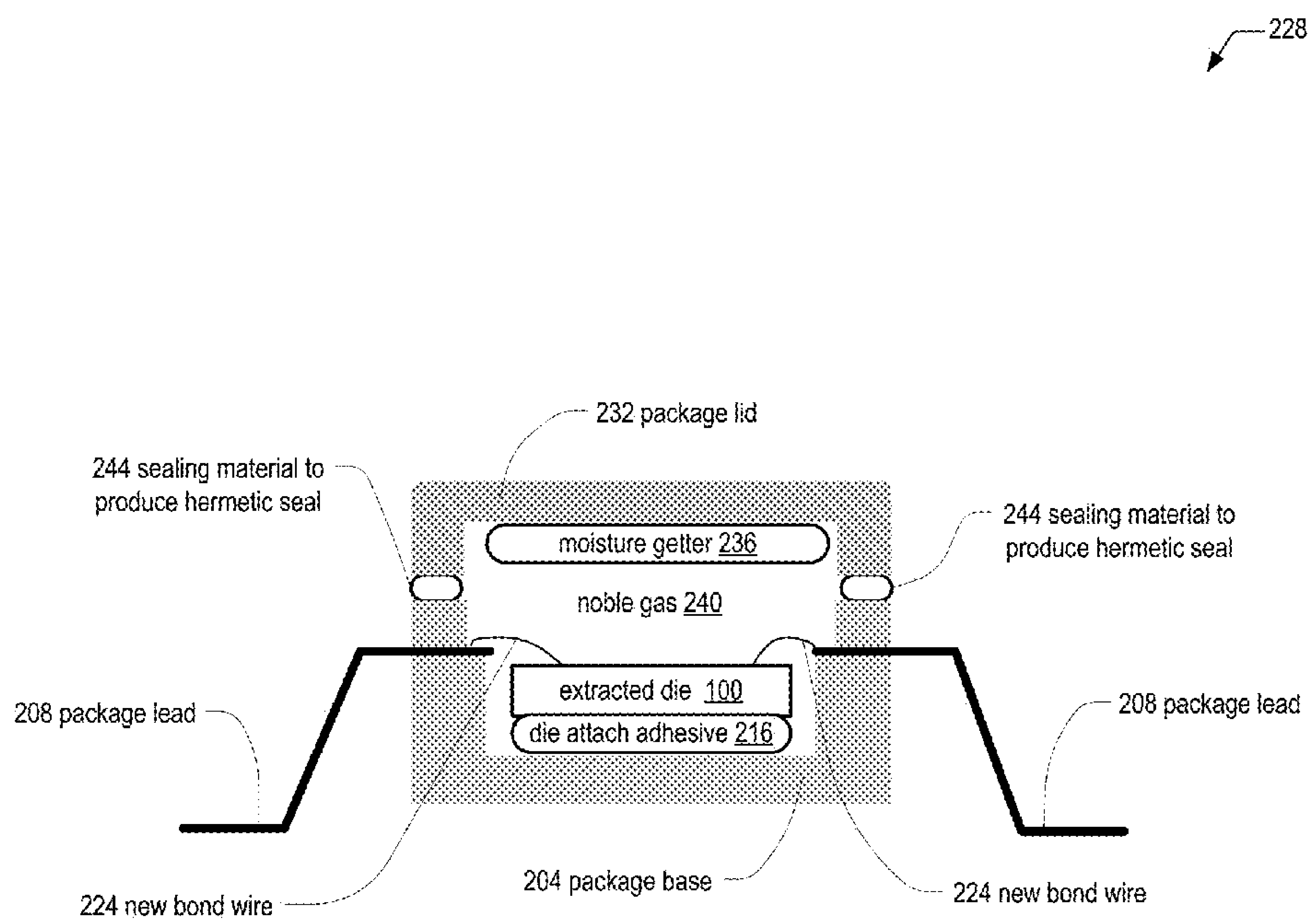


FIG. 3A Extracted die section A-A

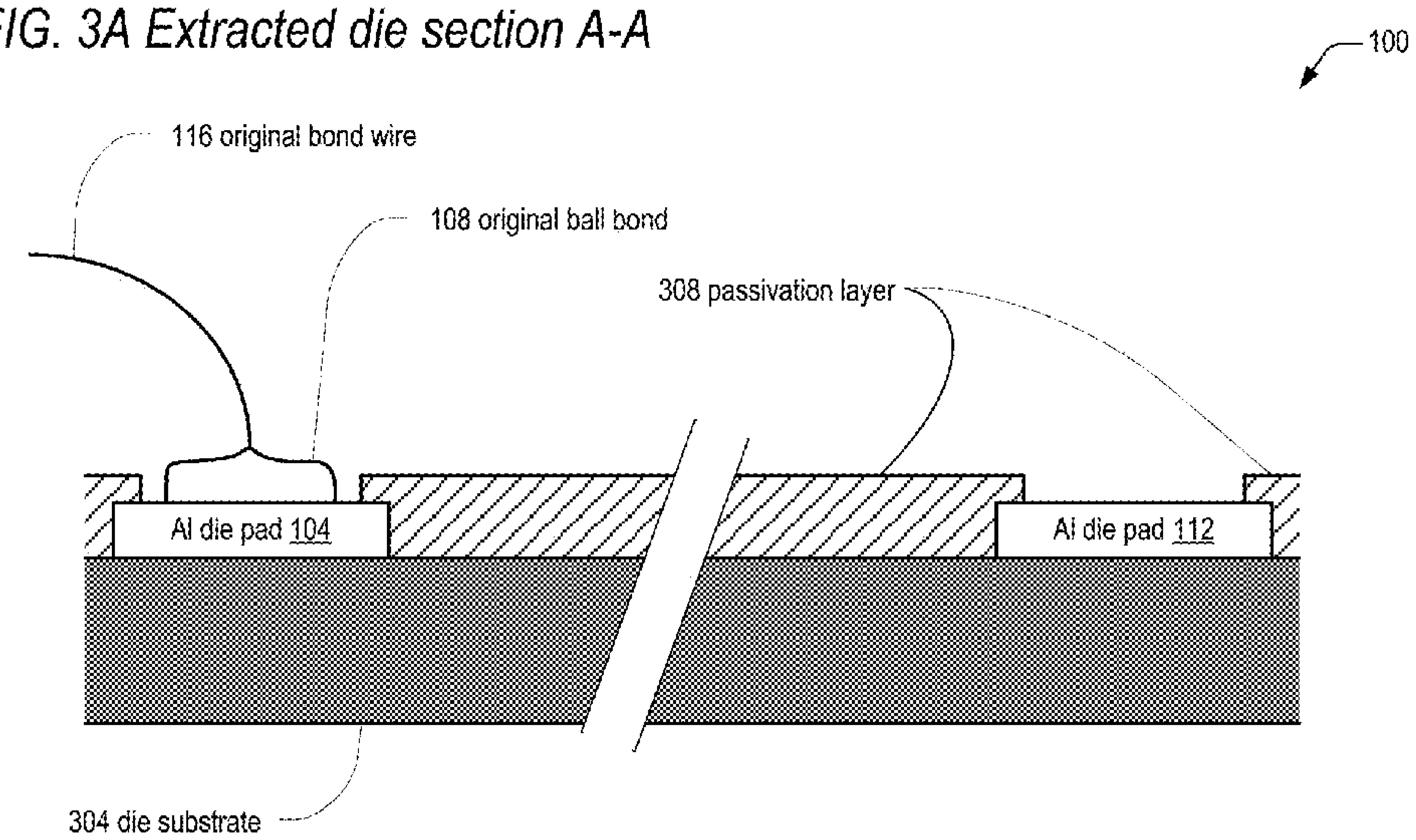


FIG. 3B Modified extracted die section A-A after original ball bond and original bond wire removal

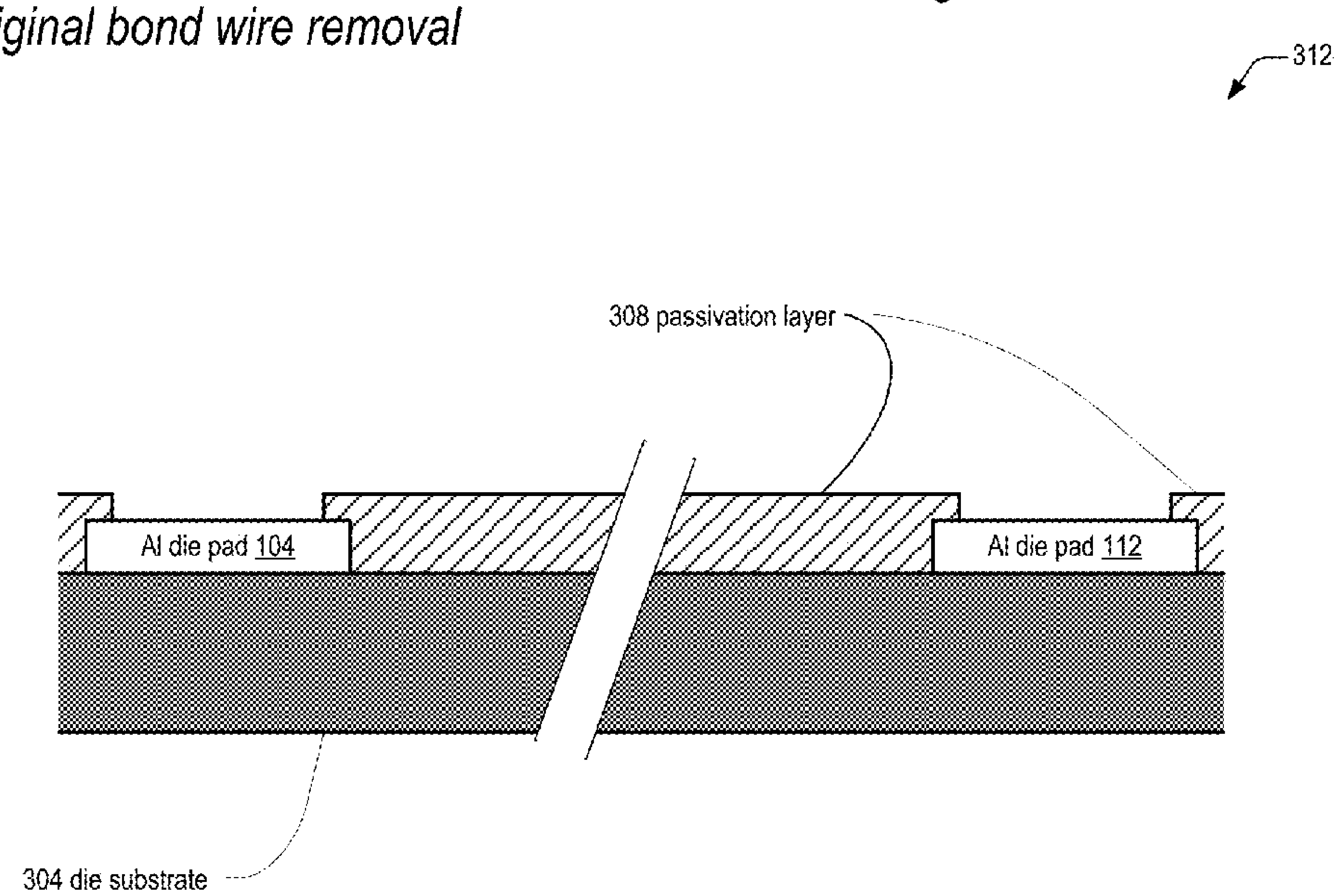


FIG. 3C Electroless Nickel layer application section A-A

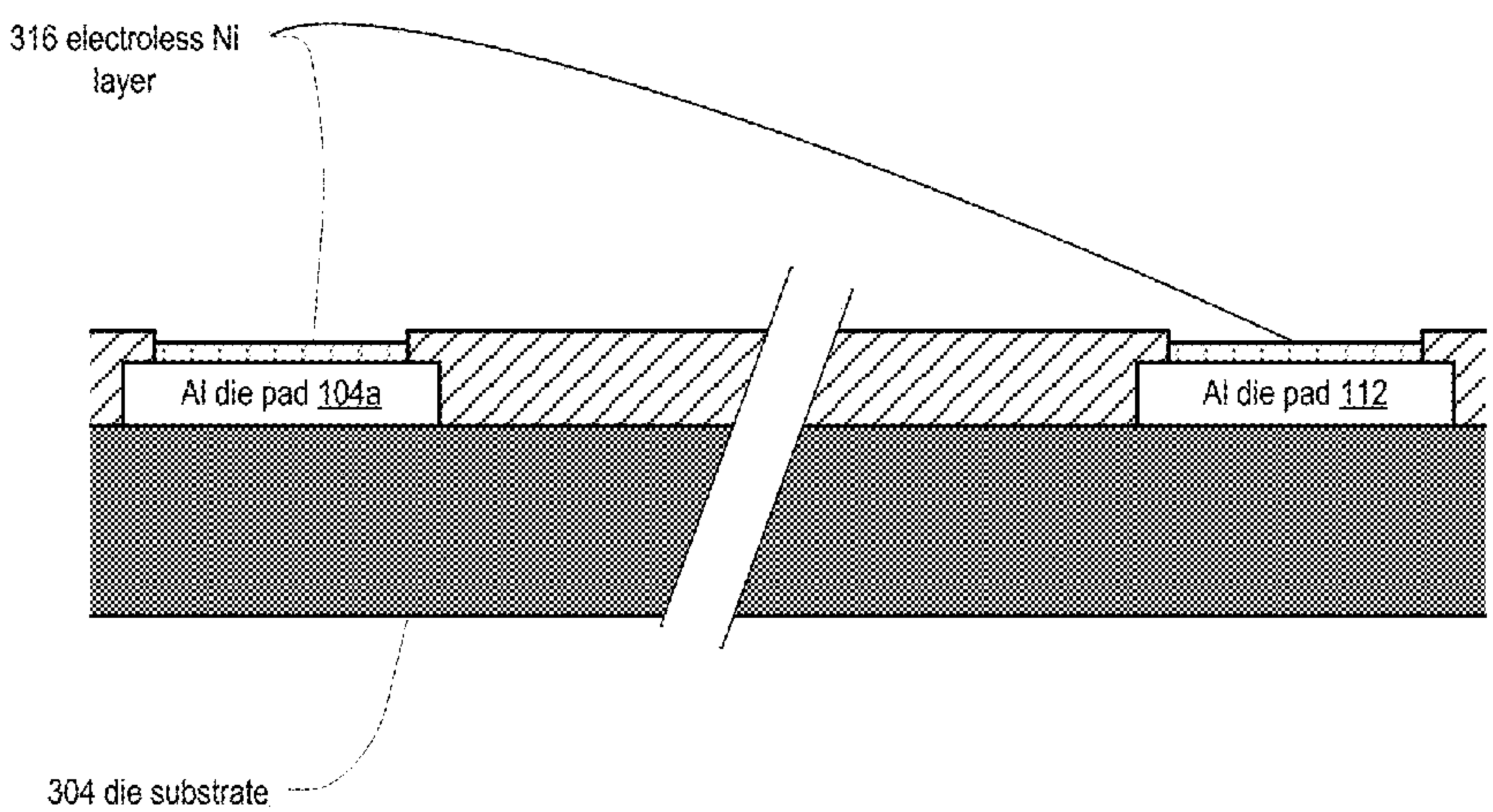


FIG. 3D Electroless Palladium layer section A-A

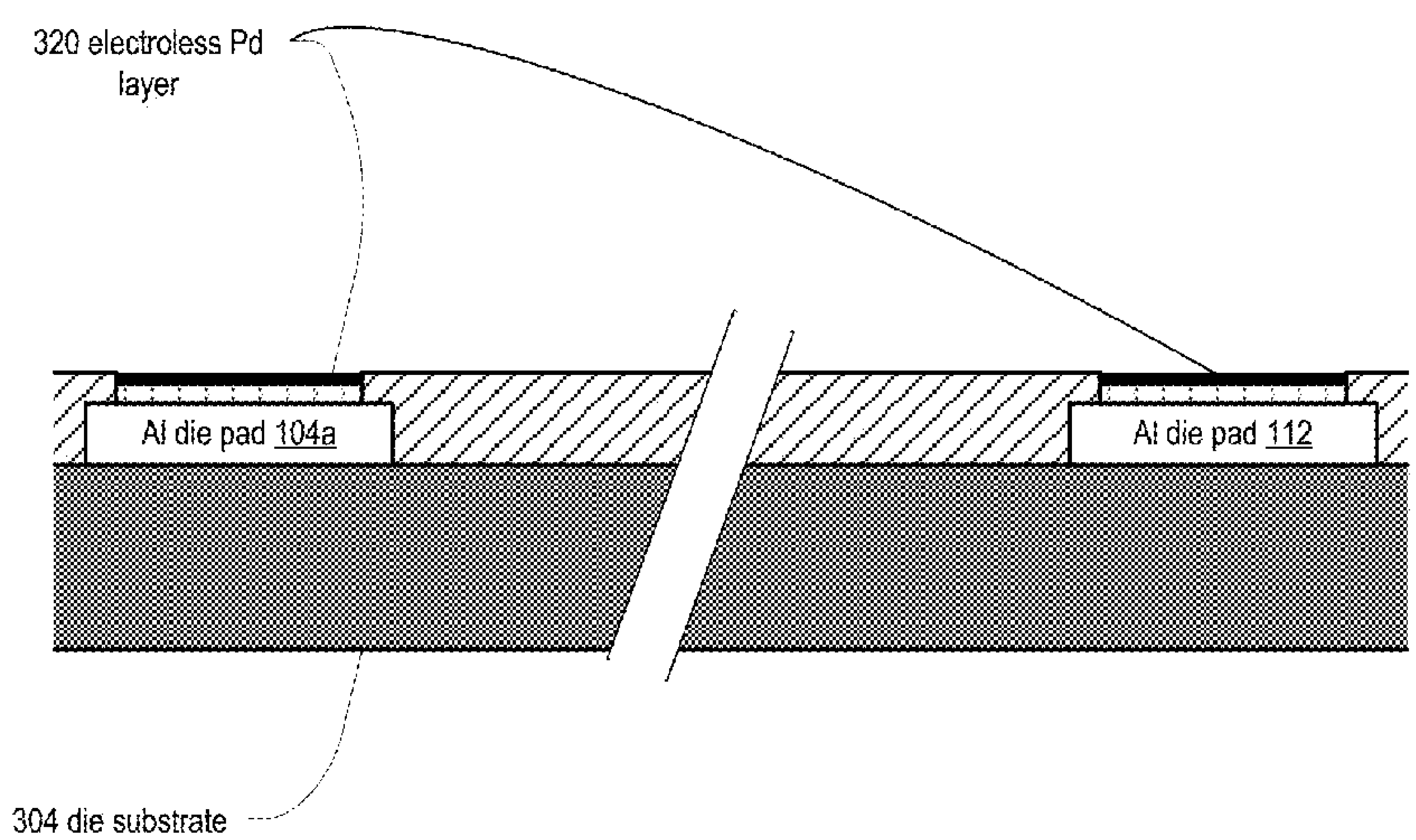


FIG. 3E Immersion Gold layer application section A-A

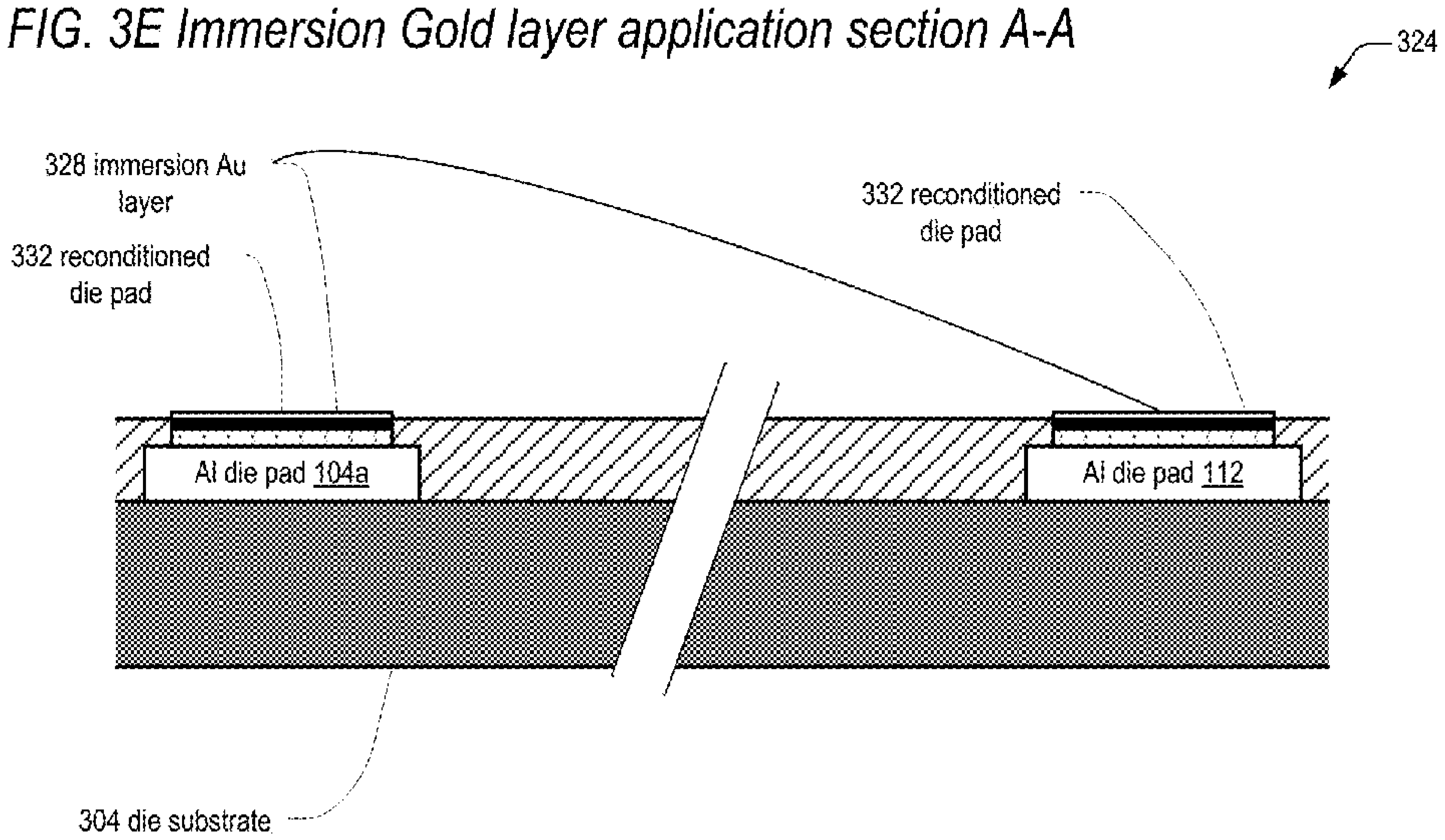


FIG. 3F New bond wire and ball bonds section A-A

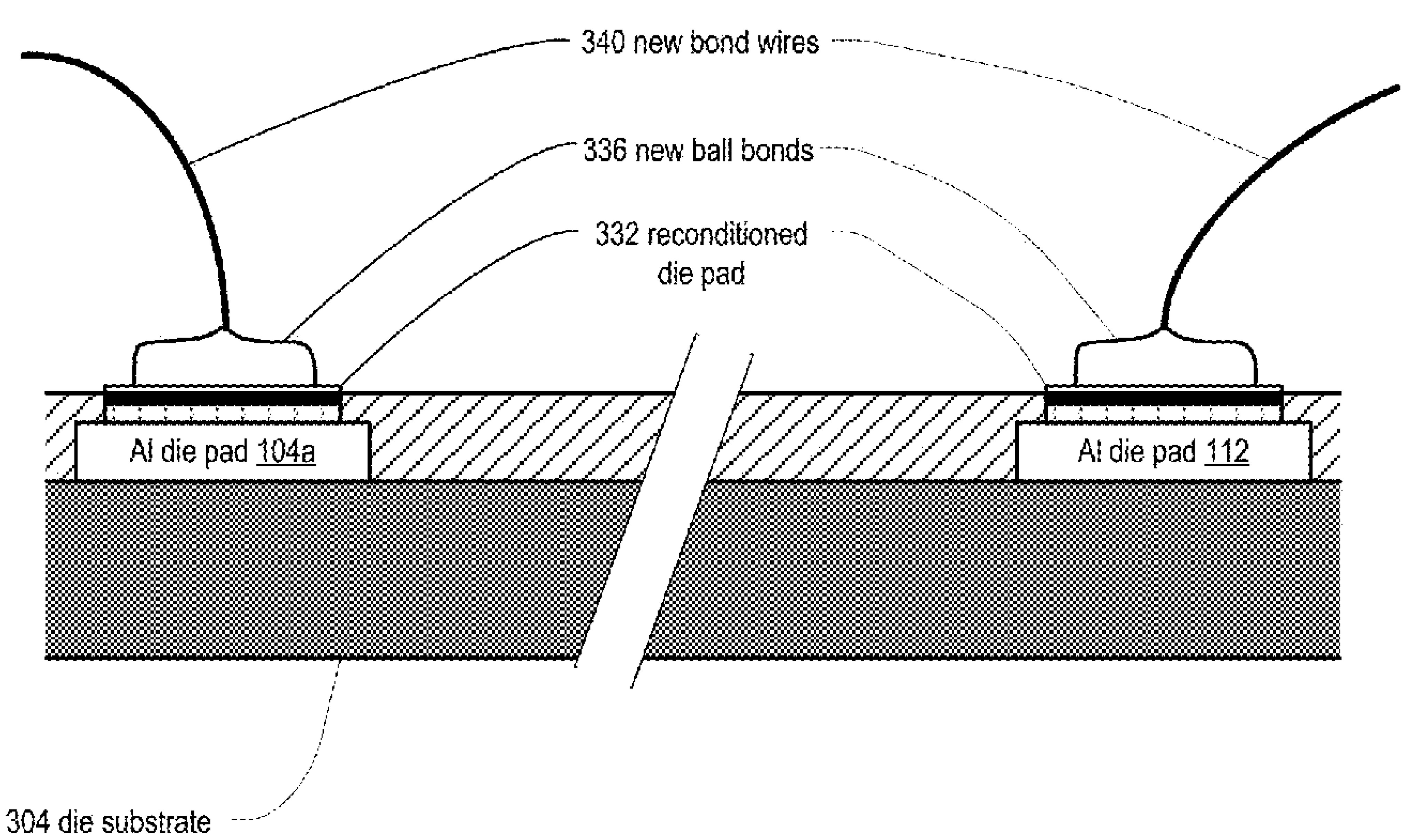


FIG. 4A Reconditioned die installed in hermetic package base

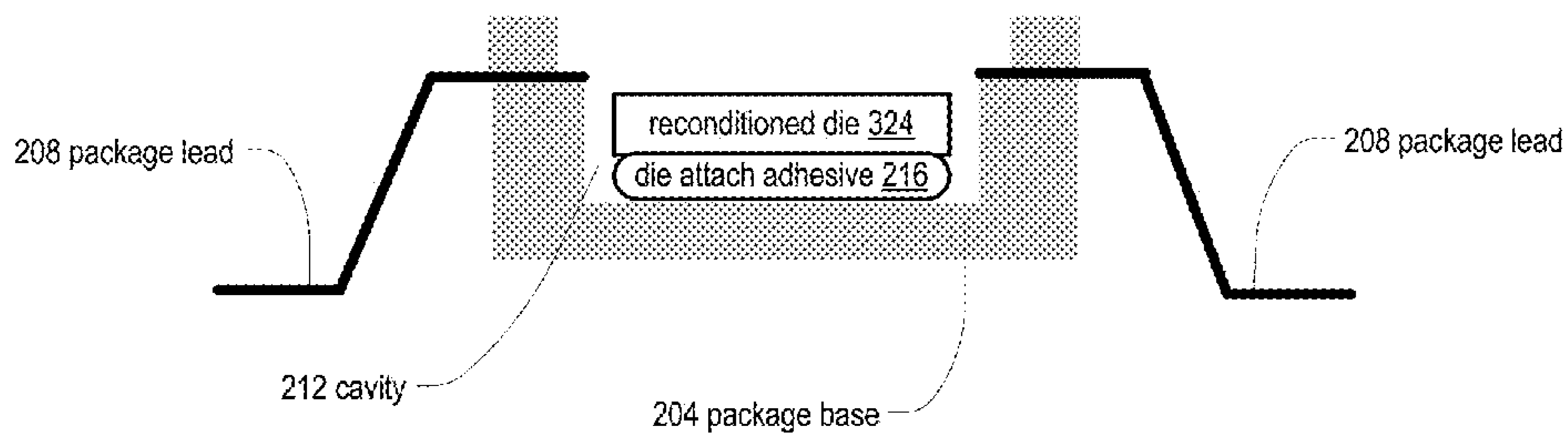


FIG. 4B Reconditioned die rebonded to package base

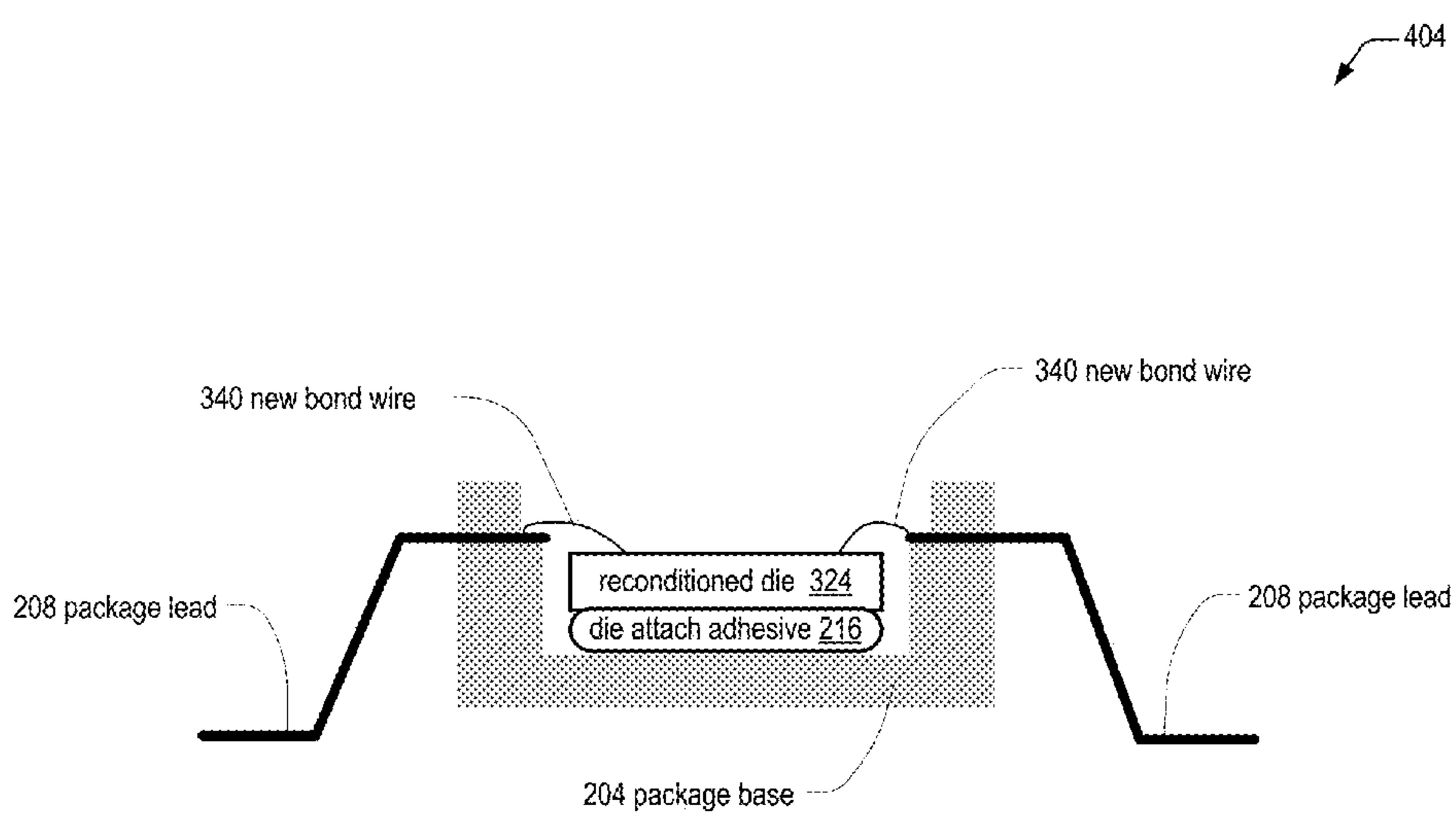


FIG. 4C Repackaged environmentally hardened integrated circuit

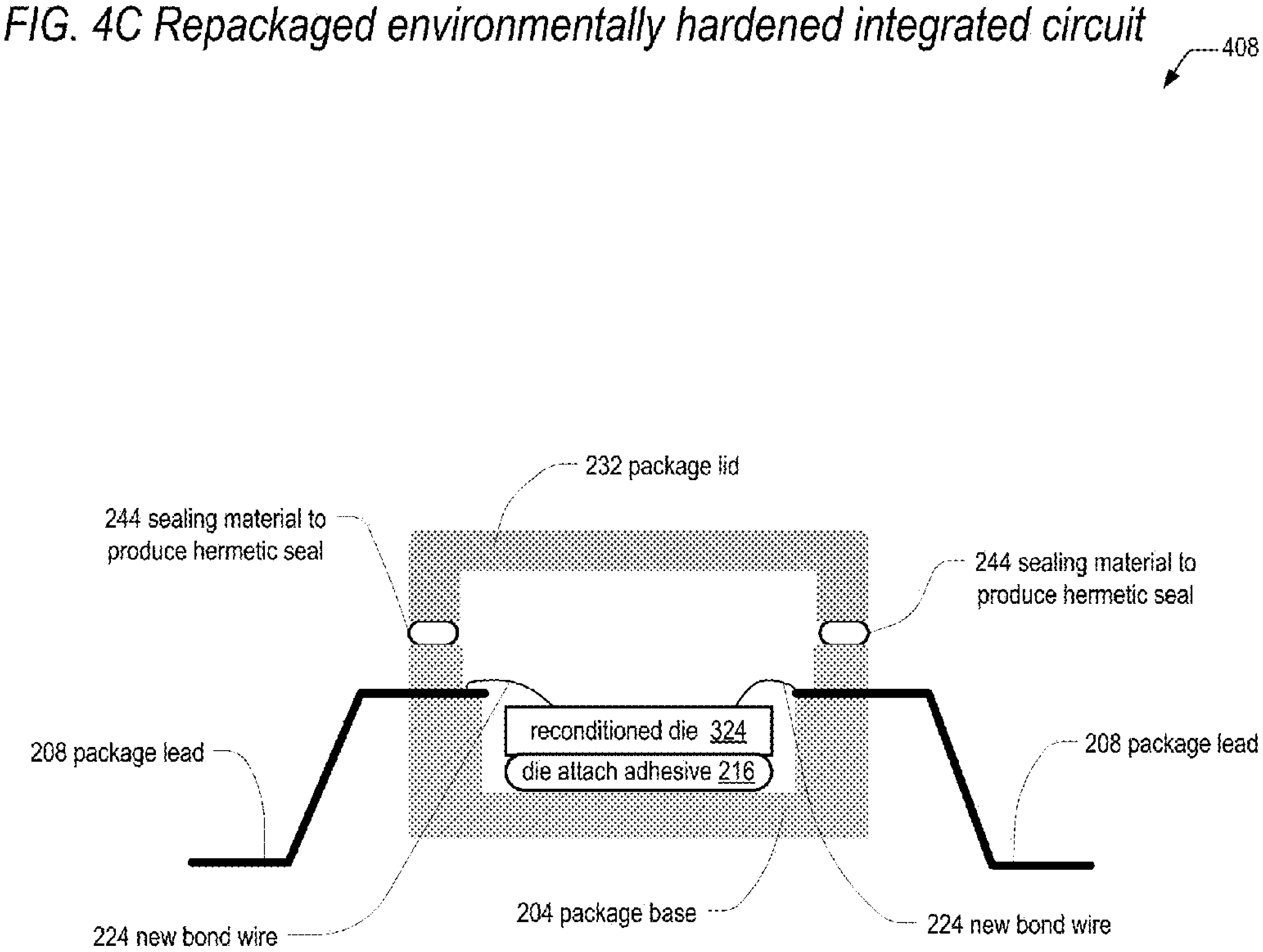


FIG. 5A Reconditioning method for extracted die

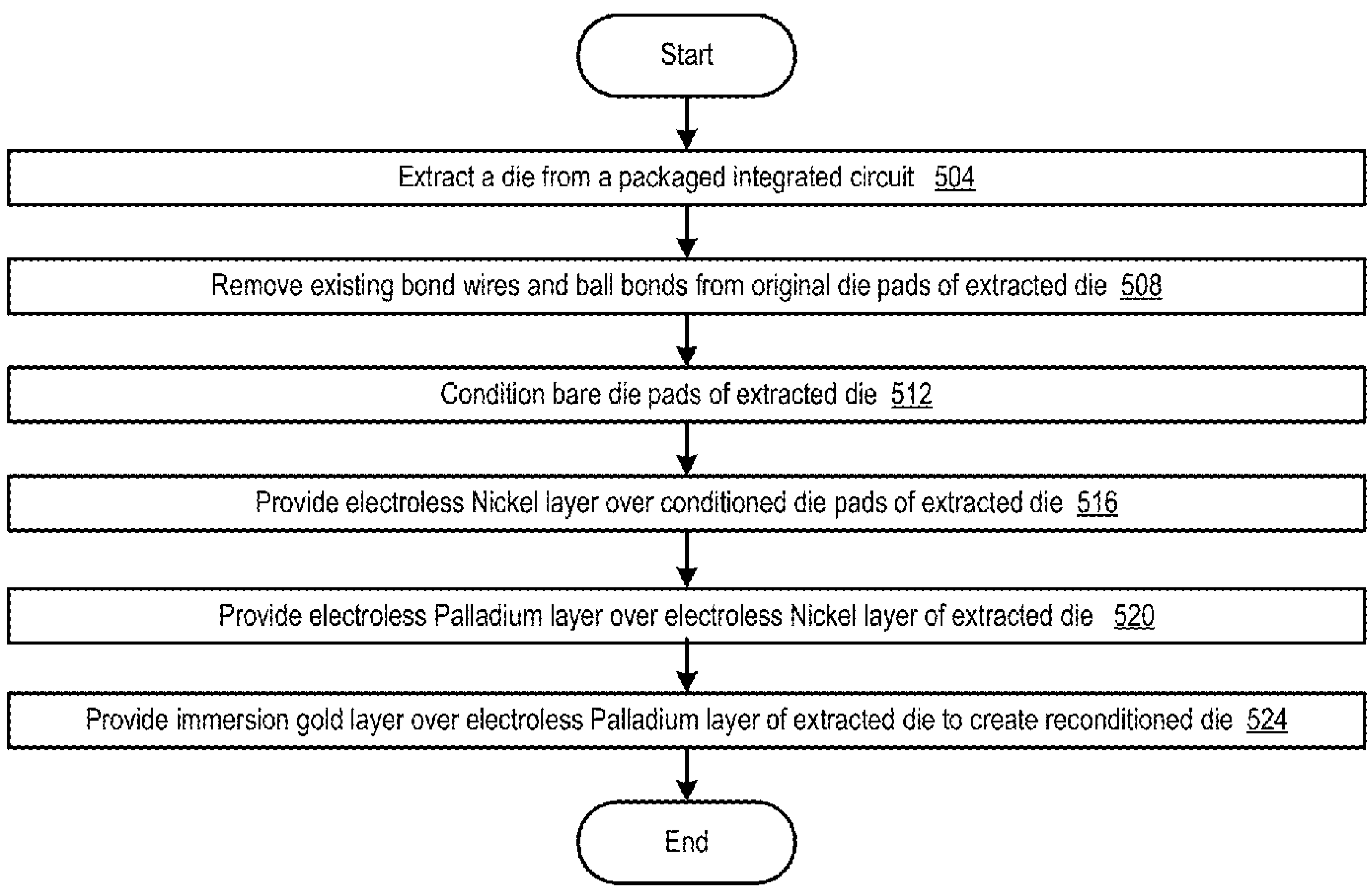


FIG. 5B Reconditioning method for extracted die

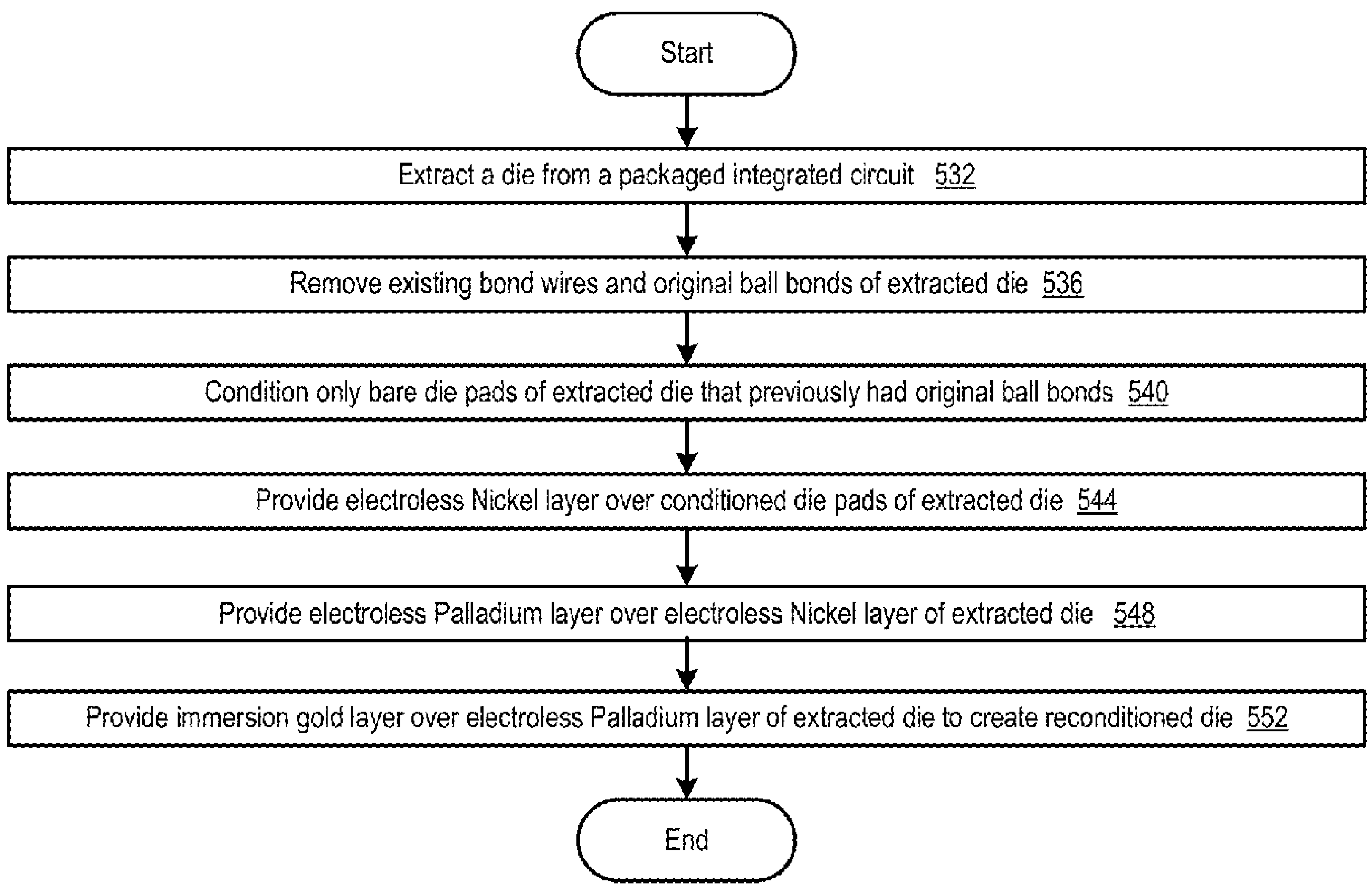
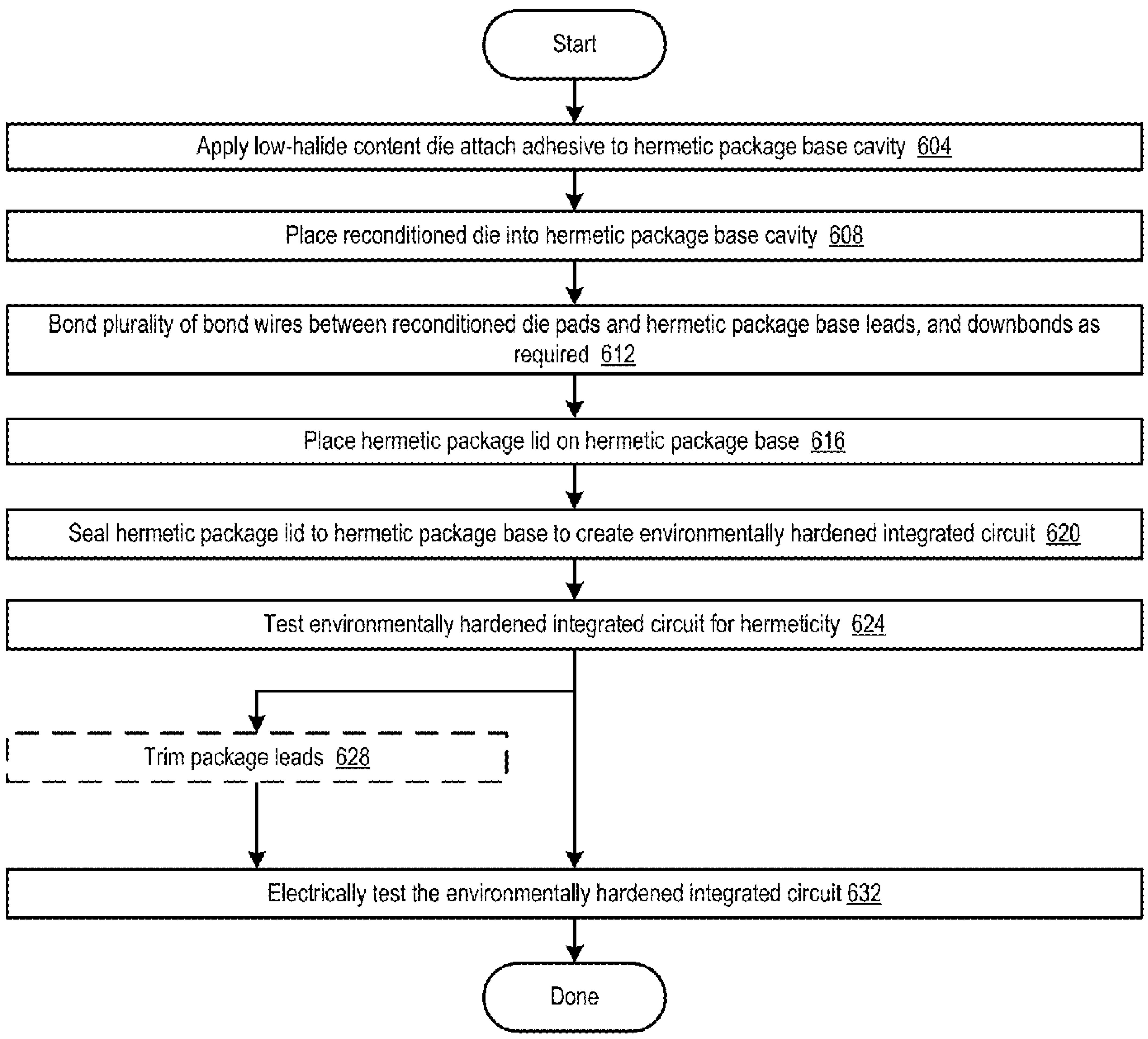


FIG. 6 Assembly method for repackaged environmentally hardened integrated circuit



REPACKAGED INTEGRATED CIRCUIT AND ASSEMBLY METHOD

CROSS REFERENCE TO RELATED APPLICATION(S)

This application is a Continuation-in-Part of pending non-Provisional U.S. application Ser. No. 13/623,603 filed Sep. 20, 2012, entitled ENVIRONMENTAL HARDENING TO EXTEND OPERATING LIFETIMES OF INTEGRATED CIRCUITS AT ELEVATED TEMPERATURES, which is hereby incorporated by reference for all purposes, which is a Continuation of U.S. application Ser. No. 13/283,293 filed Oct. 27, 2011, entitled ENVIRONMENTAL HARDENING TO EXTEND OPERATING LIFETIMES OF INTEGRATED CIRCUITS AT ELEVATED TEMPERATURES, now abandoned.

FIELD

The present invention is directed to integrated circuit packaging. In particular, the present invention is directed to methods and apparatuses for repackaging integrated circuits capable of operating at extended temperatures over extended lifetimes.

BACKGROUND

Integrated circuits are available in many different packages, technologies, and sizes. Most integrated circuits are available in plastic packages, which are generally intended for commercial operating environments at a low cost. Commercial operating environments have a specified operating range from 0° C. to 70° C. Integrated circuits for military applications have historically been packaged in either metal or ceramic hermetic packages, which are able to work reliably in more demanding environments than commercial integrated circuits. Military operating environments have a specified operating range from −55° C. to 125° C. In order to save costs, the military has purchased integrated circuits through COTS (Commercial Off-The-Shelf) programs. However, these components are generally commercial grade components in plastic packages, and not intended for demanding environments requiring the broader temperature range reliability and durability of ceramic and metal hermetically packaged integrated circuits.

Depending on size and complexity, integrated circuits are available in a wide range of packages. Although many older integrated circuits were packaged using through-hole technology packages, surface mount packages have dominated over the past several decades. Surface mount packages generally have circuit density, cost, and other advantages over through-hole integrated circuits. Examples of through-hole packages include DIP (dual-in-line plastic) and PGA (pin grid array). Examples of surface mount packages include SOIC (small-outline integrated circuit) and PLCC (plastic leaded chip carrier).

In many cases, products requiring integrated circuits are in production or service for a longer time period than the manufacturing lifetime of a given integrated circuit. In such cases, it is not uncommon for parts to become obsolete or become unable to be purchased. For example, in a typical month, about 3% of all packaged integrated circuit product types become obsolete. One mitigating approach to this issue is to buy a sufficient lifetime inventory of spares for integrated circuits that are likely to become obsolete at a future date. However, this may be costly if a large quantity of integrated circuits needs to be purchased as spares. It also may result in far more spares being purchased that are actually required, since projected future needs may only be a rough estimate. When spares are needed in the future when an IC is no longer in active production, the ICs that are actually available may be in a different package than is required, since popular ICs are typically offered in multiple package options. For example, spares may be available in plastic DIP packages while the using assemblies require SOIC packages.

SUMMARY

The present invention is directed to solving disadvantages of the prior art. In accordance with embodiments of the present invention, a packaged integrated circuit for operating reliably at elevated temperatures is provided. The packaged integrated circuit includes a reconditioned die, which includes a fully functional semiconductor die that has been previously extracted from a different packaged integrated circuit. The packaged integrated circuit also includes a hermetic package comprising a base and a lid and a plurality of bond wires. The reconditioned die is placed into a cavity in the base. After the reconditioned die is placed into the cavity, the plurality of bond wires are bonded between pads of the reconditioned die and package leads of the hermetic package base or downbonds. After bonding the plurality of bond wires, the lid is sealed to the base.

In accordance with another embodiment of the present invention, a method for assembling a packaged integrated circuit for operating reliably at elevated temperatures is provided. The method includes extracting a die from a different packaged integrated circuit, where the extracted die is a fully functional semiconductor die. The method also includes reconditioning the extracted die including adding a sequence of metallic layers to bare die pads of the extracted die, placing the reconditioned die into a cavity of a hermetic package base, bonding a plurality of bond wires between pads of the reconditioned die to leads of the hermetic package base or downbonds and sealing a hermetic package lid to the hermetic package base.

In accordance with a further embodiment of the present invention, a packaged integrated circuit for operating reliably at elevated temperatures is provided. The packaged integrated circuit includes an extracted die, where the extracted die is a fully functional semiconductor die that has been previously removed from a different packaged integrated circuit. The packaged integrated circuit also includes a hermetic package including a base and a lid, and a plurality of bond wires. After removing bond wires from the extracted die, a sequence of metallic layers is applied over the existing ball bonds and die pads of the extracted die to produce a reconditioned die and the reconditioned die is placed into a cavity in the hermetic package base. After the reconditioned die is placed into the cavity, the plurality of bond wires are bonded between pads of the reconditioned die and package leads of the hermetic package base or downbonds. After bonding the plurality of bond wires, the hermetic package lid is sealed to the hermetic package base.

An advantage of the present invention is that it provides an improved packaged integrated circuit that works reliably at extended ambient temperatures. Packaged integrated circuits of the conventional art require components and assembly steps that take longer and add cost relative to the present invention. Therefore, the former methods are less suitable for volume production.

Yet another advantage of the present invention is it provides high temperature-tolerant packaged integrated circuits without requiring new bare dice. Often, new bare dice are not available due to integrated circuit obsolescence, the original manufacturer or foundry is out of production, or the dice manufacturer is only selling packaged integrated circuits. By using extracted dice as the source, as long as the dice are available in some package, they may then be re-used in high-temperature hermetic packages.

One additional advantage of the present invention is that it allows an existing component to be repackaged into virtually any possible hermetic package and reused. Sometimes, the only available components are packaged in commercial plastic packages, but the using application requires a specific different hermetic package. As long as the specific different hermetic package is available, the die in the original commercial package may be repackaged in the specific different hermetic package.

Additional features and advantages of embodiments of the present invention will become more readily apparent from the following description, particularly when taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram illustrating an extracted die with bond pads and ball bonds in accordance with embodiments of the present invention.

FIG. **2**A is a diagram illustrating an extracted die installed in a hermetic package base in accordance with the present invention.

FIG. **2**B is a diagram illustrating an extracted die rebonded to a hermetic package base in accordance with the present invention.

FIG. **2**C is a diagram illustrating a repackaged environmentally hardened integrated circuit in accordance with the present invention.

FIG. **3**A is a diagram illustrating a section A-A of an extracted die in accordance with embodiments of the present invention.

FIG. **3**B is a diagram illustrating a section A-A of a modified extracted die after original ball bond and original bond wire removal in accordance with embodiments of the present invention.

FIG. **3**C is a diagram illustrating a section A-A of electroless nickel layer application in accordance with embodiments of the present invention.

FIG. **3**D is a diagram illustrating a section A-A of electroless palladium layer application in accordance with embodiments the present invention.

FIG. **3**E is a diagram illustrating a section A-A of immersion gold layer application in accordance with embodiments the present invention.

FIG. **3**F is a diagram illustrating a section A-A of new bond wire and ball bonds in accordance with embodiments the present invention.

FIG. **4**A is a diagram illustrating a reconditioned die installed in a hermetic package base in accordance with the preferred embodiment of the present invention.

FIG. **4**B is a diagram illustrating a reconditioned die rebonded to a package base in accordance with the preferred embodiment of the present invention.

FIG. **4**C is a diagram illustrating a repackaged environmentally hardened integrated circuit in accordance with the preferred embodiment of the present invention.

FIG. **5**A is a flowchart illustrating a reconditioning method for an extracted die in accordance with a first embodiment of the present invention.

FIG. **5**B is a flowchart illustrating a reconditioning method for an extracted die in accordance with a second embodiment of the present invention.

FIG. **6** is a flowchart illustrating an assembly method for a repackaged environmentally hardened integrated circuit in accordance with the preferred embodiment of the present invention.

DETAILED DESCRIPTION

Many operating environments require integrated circuit components capable of operating reliably at extended temperatures. Some of these environments include engine controls, down-hole drilling, and foundry manufacturing operations. Engine controls are often located in close proximity to an internal combustion, gas turbine, or jet engine, and are sometimes located on the engine side of a firewall. Down-hole drilling requires a wide variety of sensors, control components, and communication components operating in close proximity to a drill. In addition to heat generated by the drill itself, drilling far below the Earth's crust can reach operating environment temperatures of greater than 200° C. due to geothermal heat. Foundry operations require sensors and control components operating in close proximity to molten metal.

Although military grade integrated circuits are often desirable for extended high temperature environments, in many cases the environments themselves experience higher temperatures than the military grade integrated circuit temperature rating. For example, down-hole drilling environments sometimes reach temperatures of 250° C., while military-grade integrated circuits commonly have a −55° C. to 125° C. operating temperature range. Another problem is the required integrated circuits may not be available in packages that can reliably withstand these temperature extremes. Required integrated circuits are sometimes out of production, and it is typically prohibitively expensive to procure new integrated circuits in suitable packaging. Therefore, what is needed is a method for modifying existing integrated circuits in order to work reliably at extended temperature operating environments.

Integrated circuits are most commonly packaged using dice with Aluminum (Al) bond pads and Gold (Au) bond wires from the bond pads to the package leads and package cavity. Since bare dice are generally not available, it is highly desirable to obtain dice from already packaged integrated circuits. Integrated circuit dice are then extracted from an existing package—usually plastic—and repackaged into a suitable hermetic package according to the methods of the present invention. These extracted dice retain the original Au ball bonds on the Al die pads.

Several known failure mechanisms exist with Au—Al metallic interfaces. A brief overview is discussed in Wikipedias "Gold-aluminum intermetallic", which can be found at: http://en.wikipedia.org/wiki/Gold-aluminium_intermetallic. A more in-depth discussion of Gold (Au)-Aluminum (Al) intermetallics can be found in "Wire Bonding in Microelectronics", Third Edition, by George Harman—published in 2010 by McGraw-Hill, ISBN P/N 978-0-07-170101-3 and CD P/N 978-0-07-170334-5 of set 978-0-07-147623-2. Specifically, the Harman reference discusses Au—Al intermetallic compounds in Chapter 5 pages 131-153, thermal degradation in Au ball bonds on Al bond pads in Appendix

5B pages 170-173, and wire bonds in extreme temperature environments in Chapter 9 pages 330-335.

Approximately 95% of all integrated circuits utilize Au ball bonds on Al bond pads, are plastic encapsulated and, are subjected to high temperatures in the resin curing process. There are five Au—Al intermetallic compounds: Au_5Al_2, Au_4Al, Au_2Al, $AuAl_2$, and AuAl. Gold-Aluminum intermetallic compound formation and associated Kirkendall voids have resulted in more documented wire-bond failures than any other integrated circuit problem over the years. The $AuAl_2$ intermetallic compounds are typically referred to as "purple plague", reflecting the characteristic color that often occurs around the perimeter of an Au bond on an Al pad. The compounds grow during the curing of plastic molding compounds (typically 175° C. for 3 to 5 hours) and grow during qualification screening, burn in, stabilization bakes, or cumulatively at any time when high temperatures (above 150° C.) are encountered during the life of the device.

Bond failures result from the formation of Kirkendall voids, as well as from the susceptibility of Au—Al couples to the degradation by impurities or corrosion. Kirkendall voids form when either the Al or Au diffuses out of one region faster than it diffuses in from the other side of that region. Vacancies pile up and condense to form voids, normally on the Au-rich side. Classical Kirkendall voids require bake times greater than an hour at temperatures greater than 300° C. to occur on the Au-rich side and greater than 400° C. on the Al-rich side, or much longer times of lower temperatures. However, the failures resulting from impurities, poor welding, hydrogen, or other defects in plated Au layers can appear to have resulted from Kirkendall voiding. It has been observed that Kirkendall voids may form more quickly over time at elevated temperatures in packaged integrated circuits in the presence of impurities, halides, and/or moisture around the Au—Al bonds. Halides present in plastic packages contribute to significantly faster formation of Kirkendall voids relative to that of hermetic packages. In plastic packages, moisture will easily travel through the plastic package and reach the die surface, mixing with present halides and causing the IC to prematurely fail. Therefore, what is needed is a process to repackage integrated circuits in such a way as to discourage the formation of Kirkendall voids and other forms of intermetallic bond weakness at elevated temperatures.

From this discussion, it can be seen that it is desirable to avoid Au—Al bonds, especially when the packaged integrated circuit incorporating these bonds is exposed to extreme environmental conditions incorporating high temperatures, high temperature gradients, and high levels of shock and vibration.

The ENEPIG surface finish (Electroless Nickel/Electroless Palladium/Immersion Gold) originated in the mid-1990s as a modification of the more conventional ENIG finish (Electroless Nickel/Immersion Gold). During development of ENEPIG, it was recognized that the addition of a Palladium (Pd) layer between the nickel (Ni) and the gold (Au) enabled both gold and aluminum (Al) wire bonding operations, in addition to the normal soldering application. In addition, the Pd layer was found to limit the corrosion of the nickel by an overly aggressive immersion gold application process. An electrolytic nickel/gold finish was typically the process of record for integrated circuit gold wire bonding applications.

As a surface finish, ENEPIG has received increased attention for gold wire bonding operations. With a lower gold thickness compared to ENIG processes, ENEPIG exhibits improved reliability, better performance, and reduced cost.

The present invention is directed to the problem of repackaging integrated circuit dice into hermetic packages able to work reliably at high temperature extremes. Once a die has been extracted from an existing integrated circuit package (also described herein as a finished packaged integrated circuit or a different packaged integrated circuit), gold ball bonds still remain on the die bond pads. In some embodiments, new bond wires are bonded between the existing balls of the extracted die and package leads and the package cavity of the new package. The new package may be the same type of package the die was extracted from, or it may be an entirely different type of integrated circuit package. However, in all cases the new package must be able to be hermetically sealed for optimum lifetime at elevated temperatures. A hermetically sealed integrated circuit is an airtight and moisture-tight integrated circuit. Integrated circuit hermeticity is specified in MIL-SPEC-883H "Department of Defense Test Method Standards Microcircuits" test method 1014.13. Hermetically sealed packages in current technology require a ceramic or metal lid and base. However, it is possible in the future that hermetically sealed packages may use a lid and base fabricated from a material other than ceramic or metal, and the present invention therefore applies to any hermetic package material.

Referring now to FIG. **1**, a diagram illustrating an extracted die **100** with bond pads and ball bonds in accordance with embodiments of the present invention is shown. In most embodiments, extracted die **100** is an individual semiconductor die or substrate, and is usually fabricated in suitable technologies including Silicon (Si) and Gallium Arsenide (GaAs). Extracted die **100** may have a single die or multiple interconnected dice. Regardless whether extracted die **100** includes a single die or multiple interconnected dice, die circuitry is connected to individual die pads **104**, **112** of the extracted die **100**. Die pads **104** are aluminum (Al) or copper (Cu) alloy pads. Each previously used die pad **104** of the extracted die **100** has an original gold ball bond **108** present, and possibly an associated original bond wire **116**. When the extracted die **100** was present in whatever previous package was used for the extracted die **100**, original bond wires **116** connected each of the original gold ball bonds **108** to a lead or a downbond of the previous package. FIG. **1** illustrates the extracted die **100**, after it has been removed from the previous package. Therefore, some original bond wires **116** have been removed and only original gold ball bonds **108** and two original bond wires **116** remain. Depending on the specific extracted die **100**, one or more unbonded die pads **112** may be present—where no original ball bond **108** and original bond wire **116** previously existed. Unbonded die pads **112** generally indicate a no connect to the previous package leads, and may or may not be connected to other circuitry of the extracted die **100**. Section A-A provides a reference to an end-on view for other drawings to illustrate the construction and methods of the present invention.

Referring now to FIG. **2A**, a diagram illustrating an extracted die **100** installed in a hermetic package base **204** in accordance with the present invention is shown. The hermetic package base **204** may be formed from ceramic, metal, or glass materials. The hermetic package base **204** includes a cavity **212** into which an extracted die **100** is placed.

Die attach adhesive **216** is applied to the hermetic package base **204** such that when the extracted die **100** is inserted into the hermetic package base cavity **212**, the die attach adhesive **216** makes simultaneous contact with both the interior of the hermetic package base **204** and the bottom surface of the extracted die **100**. Die attach adhesive **216** is a low-halide compound adhesive, where a low halide compound has less than 10 parts per million (ppm) halide. Die attach adhesive **216** therefore bonds the extracted die **100** to the hermetic package base **204**, and protects the integrity of the interior of the repackaged environmentally hardened integrated circuit. It has been well established that halogens in an Au—Al bond interface degrade Au—Al bond strength since out gassed products from adhesives containing halogens rapidly corrode Al metallization in integrated circuits at high temperatures, thus reducing product lifetime.

Associated with the hermetic package base **204** are a series of package leads **208**, which provide interconnection between circuitry of the extracted die **100** and circuitry of a printed circuit board on which the repackaged environmentally hardened integrated circuit is eventually mounted. For example, if an S0-24 ceramic package is used for the repackaged environmentally hardened integrated circuit, 24 package leads **208** would be present, configured as 12 package leads **208** on each of two opposite sides of the hermetic package base **204**. If a PLCC-68 ceramic package is used for the repackaged environmentally hardened integrated circuit, 68 package leads **208** would be present, configured as 17 package leads **208** on each of the four sides of the hermetic package base **204**.

Referring now to FIG. **2**B, a diagram illustrating an extracted die **100** rebonded to a hermetic package base **204** in accordance with the present invention is shown. One the rebonding is completed, the result is an assembled hermetic package base **220**. After mounting the extracted die **100** into the hermetic package base **204** using die attach adhesive **216**, bond wires **224** are then attached by thermosonic welding from original gold ball bonds **108** of extracted die **100** to package leads **208**. Thermosonic welding utilizes ultrasonic and thermal energy to provide strong bonds between bond wires **224** and die pads **104**/package leads **208**. Bond wires **224** are commonly 1-3 mils in diameter, but may be any usable diameter. In a preferred embodiment, bond wires **224** are Gold (Au) bond wires **224**. In other embodiments, bond wires **224** are Aluminum (Al) or Copper (Cu) bond wires **224**.

Once all new bond wires **224** are bonded between package leads **208** and original gold ball bonds **108** or downbonds to the package cavity **212**, the assembled hermetic package base **220** including extracted die **100**, die attach adhesive **216**, hermetic package base **204**, package leads **208**, and new bond wires **224** is first vacuum baked according to the processes disclosed in related application Ser. No. 13/623,603. The assembled hermetic package base **220** is an intermediate assembly of the repackaged environmentally hardened integrated circuit **228** illustrated in FIG. **2***c*.

Referring now to FIG. **2**C, a diagram illustrating a repackaged environmentally hardened integrated circuit **228** in accordance with the present invention is shown. Repackaged environmentally hardened integrated circuit **228** includes the assembled hermetic package base **220** of FIG. **2***b* and additional components described below.

Following the first vacuum baking process of application Ser. No. 13/623,603, a hermetic package lid **232** is attached to the assembled hermetic package base **220**. The hermetic package lid **232** may be formed from ceramic, metal, or glass materials.

A moisture getter **236** is present within the repackaged environmentally hardened integrated circuit **228**. The moisture getter **236** is a compound that absorbs moisture within the repackaged environmentally hardened integrated circuit **228** after the package has been hermetically sealed. By absorbing moisture that rapidly weakens Au—Al bonds at temperatures over 175° C., the predominant high temperature failure mechanism is minimized within the repackaged environmentally hardened integrated circuit **228**. An example of a moisture getter **236** is Cookson Group STAY-DRY® SD1000, which is a paste formulation high-temperature moisture getter **236** intended for high reliability applications. In a preferred embodiment, moisture getter **236** is applied to the interior surface of the hermetic package lid **232** using a deposition process, where uniform thickness of three or more microns of moisture getter **236** is applied.

A sealing material **244** is present between the hermetic package base **204** and the hermetic package lid **232** to produce a hermetic seal at the end of a second vacuum bake process. The second vacuum bake process is illustrated and further described in application Ser. No. 13/623,603 as well. In a preferred embodiment, sealing material **244** is applied to the hermetic package lid **232** prior to attaching the hermetic package lid **232** to the assembled hermetic package base **220**. In one embodiment, the sealing material **244** is sealing glass. In another embodiment, the sealing material **244** is an epoxy. In a third embodiment, the sealing material **244** is a solder compound.

In conjunction with the second vacuum bake process, a noble gas **240** is injected into the interior of the repackaged environmentally hardened integrated circuit **228**. Noble gas **240** injection occurs prior to sealing the hermetic package lid **232** to the assembled hermetic package base **220**, but during the second vacuum bake process. In a preferred embodiment, the noble gas **240** is Argon. In other embodiments, noble gas **240** includes any one of Helium (He), Neon (Ne), Krypton (Kr), Xenon (Xe), and Radon (Rn). Noble gases **240** pressurize the repackaged environmentally hardened integrated circuit **228** such that over temperatures of −55° C. to 250° C., the internal pressure of the repackaged environmentally hardened integrated circuit **228** is maintained between 0.1 ATM and 2 ATM, preferably 1 ATM. This minimizes pressure-caused stress to the repackaged environmentally hardened integrated circuit **228**, and especially stress to the sealing material **244**. Noble gases **240** are used in preference to other gases since noble gases **240** are inert and do not react with the moisture getter **236**. In a preferred embodiment, the noble gas **240** is injected into the cavity to a pressure of between 0.1 to 2 Atmospheres (ATM), preferably 1 ATM, at a temperature between 200° C. and 275° C., preferably 255° C.

Although the steps and components illustrated in FIG. **2***a*-**2***c* will produce a highly reliable hermetic packaged integrated circuit **228**, it should be noted that the moisture getter **236** and noble gas **240** in addition to the first and second vacuum bake processes increase the fabrication time and cost of the hermetic packaged integrated circuit **228**. Therefore, it is desirable to not be required to utilize those components and processes if a reliable hermetic packaged integrated circuit **228** can be assembled otherwise.

Referring now to FIG. **3**A, a diagram illustrating a section A-A of an extracted die **100** in accordance with embodiments of the present invention is shown. In order to show the steps of the preferred embodiment of the present invention, an improvement to the process illustrated in FIGS. **2***a*-**2***c*, a side view of the extracted die **100** is provided.

Extracted die **100** includes a die substrate **304** including various metallization layers known in the art. On the surface of the die substrate **304** are one or more Aluminum (Al) die pads **104**, **112**. A passivation layer **308** is applied over the die substrate **304** in order to protect the circuits of the die substrate **304**, and the passivation layer **308** is relieved at each of the original die pads **104**, **112** in order to provide bonding access.

Where original ball bonds **108** and original bond wires **116** are applied to original die pads **104**, **112**, the die pads are die pads **104**. Where no original ball bonds **108** and original bond wires **116** are applied to original die pads **104**, **112**, the die pads are die pads **112**. FIG. **3***a* illustrates the point at which the extracted die **100** has been removed from its' original package and one or more original ball bonds **108** and original bond wires **116** are present.

Referring now to FIG. **3**B, a diagram illustrating a section A-A of a modified extracted die **312** after original ball bond **108** and original bond wire **116** removal in accordance with embodiments of the present invention is shown. A modified extracted die is an extracted die **100** with the original ball bonds **108** and original bond wires **116** removed. Although in some embodiments original gold ball bonds **108** may be removed by mechanical means, in most cases it is preferable to use chemical removal means by known processes. FIG. **3***b* illustrates the original ball bond **108** and original bond wire **116** removed from the original die pad **104**. Not shown in FIG. **3***b* is that after removing the original ball bond **108** and original bond wire **116**, some amount of intermetallic residue will be present on the original die pads **104**. This generally requires removal to make sure there are no impurities or residue on the original die pads **104**, **112**. The residue removal is referred herein as conditioning the die pads **104**, **112**. Removal is preferably performed using a mild acid wash. The acid wash is followed by an acid rinse that removes surface oxides present on the original die pads **104**, **112**. For plating on an Aluminum surface, a Zincate process is used to etch away a very fine layer of Aluminum from the die pads **104**, **112** and redeposit a layer of Zinc (Zn) on the die pads **104**, **112**. The fine layer of Zinc will then act as a catalyst for the Nickel plating to follow.

Once in a clean and flat state, the original die pads **104**, **112** are considered bare die pads and are ready to be reconditioned. Reconditioning of the present invention is a process whereby the original die pads **104**, **112** are built up by successive and ordered application of specific metallic layers prior to new wire bonding processes.

In one embodiment, after an extracted die **100** is removed from a packaged integrated circuit, only original bond wires **116** are removed—thus leaving original ball bonds **108** on less than all original die pads **104** of the extracted die **100**. Original ball bonds **108** must be removed prior to reconditioning original die pads **104**. Therefore, in some embodiments the metallic layers of the present invention are provided not to empty die pads **112**, but rather original die pads **104** following original ball bond **108** removal.

Referring now to FIG. **3**C, a diagram illustrating a section A-A of electroless nickel layer **316** application in accordance with embodiments of the present invention is shown. Electroless plating is more cost effective than electroplating since it does not require expensive photolithography and etch processes. However, electroless processes generally require thicker metal layers for good bondability.

A Nickel (Ni) layer **316** applied over a conditioned conventional Aluminum (Al) bond pad **104**, **112** have been found to protect pad surfaces. Nickel possesses a much higher elastic modulus than either Copper (Cu) or Aluminum (Al), which leads Nickel to have high stiffness and fracture toughness and resist deflection and absorb energy during ball bonding processes. Thus, Nickel is a preferred metallic layer **316** for the initial layer application following original die pad **104**, **112** conditioning.

An electroless Nickel plating bath is very complex and contains more chemicals (i.e. reducing agents, complexant or chelating agents, stabilizers, etc) than the Nickel source alone. These bath components perform specific functions during the chemical reaction. They are important in order to obtain a good quality Nickel deposit and must be monitored carefully during processing.

The plating rate of Nickel is a controllable parameter during the plating process, which in turn affects the final surface roughness. A fast plating rate will obviously increase the process throughput, but fast plating rates can also result in a rougher Nickel finish. Therefore, a careful balance must be maintained between processing speed and surface quality. If the Nickel surface is too rough, the next successive metal layers to be plated over the Nickel will follow the contours and also result in a rougher surface. Both surface hardness and roughness have a strong effect on wire bondability and bond strength. Harder and rougher surfaces are typically less bondable. For wire bonding applications, the electroless Nickel layer **316** is generally 120-240 microinches thick.

Referring now to FIG. **3**D, a diagram illustrating a section A-A of electroless Palladium layer **320** application in accordance with embodiments of the present invention is shown. Electroless Palladium (Pd) **320** is applied over the electroless Nickel (Ni) **316** layer of FIG. **3***c* in order to inhibit Nickel diffusion into the immersion gold layer **324** applied afterward.

Palladium plating was first investigated as a replacement for purely gold plating in order to alleviate the high cost of gold plating. Palladium and Palladium-Nickel alloys were initially developed for contact wear resistance in connector applications, but other technical advantages were identified as usage grew. Not only is a pure Palladium layer very hard, but it is also very dense which assists as a diffusion barrier. As with the electroless Nickel layer **316**, the electroless Palladium layer **320** requires a catalyst pretreatment to prepare the surface for deposition. The metal source is typically a Palladium-Ammonia compound with a hydrazine reducing agent for metal deposition. For wire bonding applications, the electroless Palladium layer **320** is generally 2-4 microinches thick, approximately 2 orders of magnitude thinner than the electroless Nickel layer **316**.

Referring now to FIG. **3**E, a diagram illustrating a section A-A of immersion Gold layer **328** application in accordance with embodiments of the present invention is shown. The immersion Gold layer **328** is applied over the electroless Palladium layer **320**, and provides the top layer of the reconditioned die pads **332**. Gold has long been a mature plating process for semiconductor applications. Two types of Gold plating processes through chemical reactions are used today: immersion and autocatalytic. Immersion Gold plating **328** is a self-limiting galvanic displacement process, where no reducing agent is required. For wire bonding applications, the electroless Gold layer **328** is generally at least 1-2 microinches thick, and preferably thicker. Following the process step of FIG. **3***e*, the die is a reconditioned die **324**.

Because the ENEPIG plating process uses gold as the wire bonding layer with gold bond wire, there is no Aluminum (Al)-Gold (Au) interface that can degrade and corrode. Thus, the ENEPIG plating process produces more reliable wire bonding interfaces and is preferred for high temperature applications over previous processes that maintained Al—Au interfaces and utilized moisture getter, noble gas insertion, and vacuum bakes to purge moisture from integrated circuit packages.

Referring now to FIG. 3F, a diagram illustrating a section A-A of new bond wire **340** and ball bonds **336** in accordance with embodiments the present invention is shown. The combination of the electroless Nickel layer **316**, electroless Palladium layer **320**, and the immersion Gold layer **328** produces a reconditioned die pad **332**. New gold bond wires **340** may be thermosonically welded to reconditioned die pads **332**, and will produce a new gold ball bond **336** at each new bond wire **340** location.

In thermosonic welding, the interface temperature is typically between 125° C. and 220° C. For ball bonding, the gold bond wire **340** is threaded through a capillary-shaped tool, and a spark melts the end of the wire forming a ball at the bottom of the tool. The bond (weld) is formed when the tool under load presses or deforms the ball against the heated bonding pad and ultrasonic energy is applied, completing the process.

Referring now to FIG. **4**A, a diagram illustrating a reconditioned die **324** installed in a hermetic package base **204** in accordance with the preferred embodiment of the present invention is shown. The illustrated assembly is an initial assembly of the repackaged environmentally hardened integrated circuit **408** illustrated in FIG. **4***c*. The assembly step illustrated in FIG. **4***a* is between the assembly processes illustrated in FIGS. **3***e* and **3***f*.

The reconditioned die **324** is installed within the cavity **212** of a hermetic package base **204**. The hermetic package base **204** may be formed from ceramic, metal, or glass materials. Die attach adhesive **216** is applied to the hermetic package base **204** such that when the reconditioned die **324** is installed into the cavity **212**, the die attach adhesive **216** makes simultaneous contact with both the hermetic package base **204** and the reconditioned die **324**. Die attach adhesive **216** is preferably a low-halide content adhesive, where a low halide compound has less than 10 parts per million (ppm) halide. However, since the preferred embodiment of the present invention lacks Al—Au metallic bonding interfaces, the effect of damaging halides is significantly reduced. Die attach adhesive **216** therefore bonds the reconditioned die **324** to the hermetic package base **204**, and protects the integrity of the interior of the repackaged environmentally hardened integrated circuit **408**.

Associated with the hermetic package base **204** are a series of package leads **208**, which provide interconnection between circuitry of the reconditioned die **324** and circuitry of a printed circuit board on which the repackaged environmentally hardened integrated circuit **408** is eventually mounted. For example, if an S0-24 ceramic package is used for the repackaged environmentally hardened integrated circuit **408**, 24 package leads **208** would be present, configured as 12 package leads **208** on each of two opposite sides of the hermetic package base **204**. If a PLCC-68 ceramic package is used for the repackaged environmentally hardened integrated circuit **408**, 68 package leads **208** would be present, configured as 17 package leads **208** on each of the four sides of the hermetic package base **204**.

Referring now to FIG. **4**B, a diagram illustrating a reconditioned die rebonded to a package base **404** in accordance with the preferred embodiment of the present invention is shown. After mounting the reconditioned die **324** into the hermetic package base **204** using die attach adhesive **216**, new gold bond wires **340** are then attached by thermosonic welding from reconditioned die pads **332** of reconditioned die **324** to package leads **208** or downbonds. Thermosonic welding utilizes ultrasonic and thermal energy to provide strong bonds between the new gold bond wires **340** and reconditioned die pads **332**/package leads **316**. New gold bond wires **340** are commonly 1-3 mils in diameter, but may be any usable diameter. In a preferred embodiment, new bond wires **340** are Gold (Au) bond wires **340**. In other embodiments, new bond wires **340** are Copper (Cu) bond wires **340**.

Referring now to FIG. **4**C, a diagram illustrating a repackaged environmentally hardened integrated circuit **408** in accordance with the preferred embodiment of the present invention is shown. Repackaged environmentally hardened integrated circuit **408** includes the assembled hermetic package base **404** of FIG. **4***b* and additional components described below.

After bonding the new gold bond wires **340** between reconditioned die pads **332** and package leads **208** or downbonds, a hermetic package lid **232** is attached to the hermetic package base **204**. The hermetic package lid **232** may be formed from ceramic, metal, or glass materials.

A sealing material **244** is present between the assembled hermetic package base **404** and the hermetic package lid **232** to produce a hermetic seal. In a preferred embodiment, sealing material **244** is applied to the hermetic package lid **232** prior to attaching the hermetic package lid **232** to the assembled hermetic package base **404**. In one embodiment, the sealing material **244** is sealing glass. In another embodiment, the sealing material **244** is an epoxy. In a third embodiment, the sealing material **244** is a solder compound. After the hermetic package lid **232** is secured to the assembled hermetic package base **404**, the repackaged environmentally hardened integrated circuit **408** is ready for electrical, functional, and/or hermeticity testing.

Referring now to FIG. **5**A, a flowchart illustrating a reconditioning method for an extracted die **100** in accordance with a first embodiment of the present invention is shown. This process converts an extracted die **100** (with original bond wires **116** and original ball bonds **108** removed) into a reconditioned die **324** of the present invention. Flow begins at block **504**.

At block **504** a die **100** is extracted from a previous packaged integrated circuit. The previous package may be a hermetic or a non-hermetic package, and in either case is discarded and not reused. The extracted die **100** is a fully functional semiconductor die that will be utilized in a new repackaged environmentally hardened integrated circuit **408**. Flow proceeds to block **508**.

At block **508**, original ball bonds **108** and original bond wires **116** attached to the original ball bonds **108** are removed from the extracted die **100** by conventional processes. Following removal of the original ball bonds **108** and associated original bond wires **116**, some metallic or chemical residues is generally on the surface of each original die pad **104**. Flow proceeds to block **512**.

At block **512**, bare die pads **104**, **112** are conditioned. Any metallic and/or chemical residues are removed from each of the original die pads **104**, **112** in order to prepare the original die pads **104**, **112** for addition of metallic layers to create a reconditioned die **324**. Removal of the residues is commonly performed using various acid washes and rinses known in the art. Following removal of the residues and drying the original die pads **104**, **112**, Flow proceeds to block **516**.

At block **516**, an electroless Nickel layer **316** is applied to each of the conditioned original die pads **104**, **112**. Application details of the electroless Nickel layer **316** were described in some detail with respect to FIG. **3***c*. Flow proceeds to block **520**.

At block **520**, an electroless Nickel Palladium layer **320** is applied to each of the die pads **104**, **112**, over the electroless Nickel layer **316**. Application details of the electroless Palladium layer **320** were described in some detail with respect to FIG. **3***d*. Flow proceeds to block **524**.

At block **524**, an immersion Gold layer **328** is applied to each of the die pads **104**, **112**, over the electroless Palladium layer **320**. Application details of the immersion Gold layer **324** were described in some detail with respect to FIG. **3***e*. Flow ends at block **524**. With the completion of adding the immersion Gold layer **328**, the die is now a reconditioned die **324** ready for assembly into a repackaged environmentally hardened integrated circuit **408**.

Referring now to FIG. **5**B, a flowchart illustrating a reconditioning method for an extracted die **100** in accordance with a second embodiment of the present invention is shown. This process converts an extracted die **100** (with only original bond wires **116** removed) into a reconditioned die **324** of the present invention. Flow begins at block **532**.

At block **532** a die **100** is extracted from a previous packaged integrated circuit. The previous package may be a hermetic or a non-hermetic package, and in either case is discarded and not reused. The extracted die **100** is a fully functional semiconductor die that will be utilized in a new repackaged environmentally hardened integrated circuit **408**. Flow proceeds to block **536**.

At block **536**, original bond wires **116** attached to the original ball bonds **108** are removed from the extracted die **100** by conventional processes. The original ball bonds **108** remain. Flow proceeds to optional block **550**.

At optional block **540**, bare die pads **112** are conditioned. Any metallic and/or chemical residues are removed from each of the original die pads **112** in order to prepare the original die pads **112** for addition of metallic layers to create a reconditioned die **324**. Removal of the residues is commonly performed using various acid washes and rinses known in the art. It is likely not feasible to condition die pads **104** since an original ball bond **108** remains on each die pad **104**. Following removal of the residues and drying the original die pads **112**, Flow proceeds to block **544**.

At block **544**, an electroless Nickel layer **316** is applied to each of the original die pads **104** with original ball bonds **108** and conditioned original die pads **112**. Application details of the electroless Nickel layer **316** were described in some detail with respect to FIG. **3***c*. Flow proceeds to block **548**.

At block **548**, an electroless Nickel Palladium layer **320** is applied to each of the die pads **104**, **112**, over the electroless Nickel layer **316**. Application details of the electroless Palladium layer **320** were described in some detail with respect to FIG. **3***d*. Flow proceeds to block **552**.

At block **552**, an immersion Gold layer **328** is applied to each of the die pads **104**, **112**, over the electroless Palladium layer **320**. Application details of the immersion Gold layer **324** were described in some detail with respect to FIG. **3***e*. Flow ends at block **552**. With the completion of adding the immersion Gold layer **328**, the die is now a reconditioned die **324** ready for assembly into a repackaged environmentally hardened integrated circuit **408**.

Referring now to FIG. **6**, a flowchart illustrating an assembly method for a repackaged environmentally hardened integrated circuit **408** in accordance with the preferred embodiment of the present invention is shown. Flow begins at block **604**.

At block **604** a low-halide content die attach adhesive **216** is applied to the hermetic package base cavity **212**. Flow proceeds to block **608**.

At block **608**, the reconditioned die **324** is placed into the hermetic package base cavity **212**. The die attach adhesive **216** acts as a glue between the reconditioned die **324** in the hermetic package base **204**, thereby adhering the reconditioned die **324** to the hermetic package base **204**. Flow proceeds to block **612**.

At block **612**, a plurality of new bond wires **340** are bonded between reconditioned die pads **332** of the reconditioned die **324** and package leads **208** as well as downbonds as required. A bond map designates the specific connections to be provided by each of the plurality of new gold bond wires **340**. Flow proceeds to block **616**.

At block **616**, the hermetic package lid **232** is placed on the assembled hermetic package base **404**. The hermetic package lid **232** is placed in proper orientation such that the combination of the hermetic package lid **232** and the assembled hermetic package base **404** is hermetically sealed. Sealing material **244** must be already in place prior to seating the lid **232** onto the assembled base **404**. Flow proceeds to block **620**.

At block **620**, the hermetic package lid **232** is sealed to the assembled hermetic package base **404** to create a repackaged environmentally hardened integrated circuit **408**. A sealing material **244** known in the art between the hermetic package lid **232** and the hermetic package base **404** is activated at a specific temperature corresponding to the type of sealing material **244** used. Flow continues to block **624**.

At block **624**, the repackaged environmentally hardened integrated circuit **408** is tested for hermeticity per MIL-SPEC-883H test method 1014.13. In one embodiment, flow proceeds to block **632**. In a second embodiment, flow proceeds to optional block **628**.

At optional block **628**, the package leads **208** are trimmed, if necessary. In some embodiments, the package leads **208** are already trimmed in the hermetic package base **204**, and do not need to be trimmed. If the package leads **208** do need to be trimmed, they are trimmed per customer requirements. Flow proceeds to block **632**.

At block **632**, the repackaged environmentally hardened integrated circuit **408** is electrically tested. Electrical testing includes forcing a fixed current through each package lead **208** and measuring the voltage of the resulting forward-biased diode, and comparing the measured voltage to the expected range. If the repackaged environmentally hardened integrated circuit **408** has passed the hermeticity and electrical tests and the package leads **208** are properly trimmed, the repackaged environmentally hardened integrated circuit **408** is marked and is a complete environmentally hardened integrated circuit ready for use. Flow ends at block **632**.

Finally, those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiments as a basis for designing or modifying other structures for carrying out the same purposes of the present invention without departing from the spirit and scope of the invention as defined by the appended claims.

The invention claimed is:

1. A packaged integrated circuit, comprising:

a reconditioned die, comprising:

a modified extracted die with reconditioned die pads, the modified extracted die comprising an extracted die with no ball bonds on die pads of the extracted die, the extracted die comprising a fully functional semiconductor die with one or more ball bonds on one or more die pads, the reconditioned die pads comprising layers of nickel, palladium, and gold over the die pads;

a package comprising package leads and configured to enclose the reconditioned die; and

a plurality of bond wires, bonded between the reconditioned die pads and the package leads or downbonds.

2. The packaged integrated circuit as recited in claim **1**, further comprising a low halide content die attach adhesive between the reconditioned die and the package, wherein the low-halide content die attach adhesive bonds the reconditioned die to a package base.

3. The packaged integrated circuit as recited in claim **1**, wherein a modified extracted die is an extracted die with ball bonds and bond wires removed, wherein reconditioned die pads comprises layers of electroless nickel, electroless palladium, and immersion gold applied to die pads of the modified extracted die.

4. The packaged integrated circuit as recited in claim **3**, wherein reconditioned die pads are only provided to die pads corresponding to die pads of the extracted die where ball bonds were present.

5. The packaged integrated circuit as recited in claim **3**, the modified extracted die further comprising no metallic residue and chemical deposits present on the surface of the die pads.

6. The packaged integrated circuit as recited in claim **1**, wherein the layer of nickel is in direct contact with the die pad and the layer of palladium is between the layer of nickel and the layer of gold.

7. The packaged integrated circuit as recited in claim **5**, wherein the packaged integrated circuit comprises one or more new ball bonds and bond wires applied over the immersion gold layer.

8. The packaged integrated circuit as recited in claim **5**, wherein the packaged integrated circuit is tested for hermeticity.

9. A packaged integrated circuit, comprising:

a reconditioned die, comprising:

a modified extracted die with reconditioned die pads, the modified extracted die comprising an extracted die with no ball bonds on die pads of the extracted die, the extracted die comprising a fully functional semiconductor die with one or more ball bonds on one or more die pads, the reconditioned die pads comprising layers of nickel, palladium, and gold over the die pads in the following sequence:

the nickel layer in direct contact with the die pads;

the palladium layer between the nickel and gold layers; and

the gold layer over the palladium layer;

a hermetic package comprising package leads; and

a plurality of bond wires, bonded between the reconditioned die pads and the package leads or downbonds.

10. The packaged integrated circuit as recited in claim **9**, wherein a low halide content die attach adhesive is between the reconditioned die and the hermetic package, wherein the low-halide content die attach adhesive bonds the reconditioned die to a hermetic package base.

11. The packaged integrated circuit as recited in claim **9**, wherein the packaged integrated circuit is tested for hermeticity per MIL-SPEC-883H test method 1014.13.

12. The packaged integrated circuit as recited in claim **9**, wherein the sequence of metallic layers covers only die pads of the modified extracted die corresponding to die pads of the extracted die that previously had existing ball bonds.

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